REMARKS/ARGUMENTS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 7-11 and 21-22 are pending in the application, with Claims 1-6 and 12-20 withdrawn from consideration, Claims 7-11 amended, and Claims 21-22 added by the present amendment.

In the outstanding Office Action, Claim 8 was rejected under 35 U.S.C. § 112, fourth paragraph; and Claims 7-11 were rejected under 35 U.S.C. § 102(b) as being anticipated by, or in the alternative under 35 U.S.C. § 103 (a) as obvious over Yamaguchi (JP 2000-068508, also U.S. Patent No. 6,169,415).

Claims 8 is amended to overcome the rejection under 35 U.S.C. § 112, fourth paragraph. Claims 7-11 are also amended to more clearly describe and distinctly claim Applicants' inventions. New Claims 21-22, dependent from Claim 8, correspond to original Claims 9 and 11, dependent from Claim 7. No new matter is added.

Briefly recapitulating, amended Claim 7 is directed to a semiconductor device evaluation apparatus that includes a calculation section configured to plot, for a plurality of insulated gate transistors with different channel lengths, an effective channel length Leff and a gate capacitance Cg (where Cg is a capacitance between a gate and a substrate) on a graph. The calculation section is also configured to extend the Leff and Cg by extrapolation on the graph. The calculation section determines gate-capacitance-vs.-effective-channel-length characteristics, and calculates a gradient A of said characteristics. The semiconductor device evaluation apparatus also includes a first determination section configured to determine a finished gate length Lg for each of the plurality of insulated gate transistors from the equation, $Lg = (Cg - Cf)/A$, by using a fringing capacitance Cf. Cf is a capacitance between

said gate and a portion of the substrate not covered with the gate, the gradient A, and the gate capacitance Cg. The semiconductor device evaluation apparatus also includes a control section configured to control the calculation section and the first determination section. Independent Claim 8 is directed to an alternative embodiment where calculation section uses a design gate length Ld instead of said effective channel length Leff. The claimed apparatus allows for easy determination of the finished gate length and prevents a measurer from being forced to expend a great deal of time and effort when measuring a large number of points.[1]

Yamaguchi discloses a technique to reduce the difference caused by the uncertainty of the threshold voltage in order to evaluate the effective channel width W_{eff}.[2] For an accurate evaluation of the effective channel width W_{eff}, a shift amount of the threshold voltage δ is introduced.[3] Thereby an accurate threshold voltage is determined from the given mask channel width and electrical characteristics, and the range of an effective cannel width W_{eff} is found accurately.[4] The structure of Yamaguchi includes a determination section 11 determines threshold voltages V_{thWi}, V_{thNa}, and virtual shift amount δ, an extraction section 12 extracts the slope f, a determination section 13 determines a true shift mount δ_0, and determination section 14 determines a channel narrowing DW (or an effective channel width W_{eff}).[5]

However, Yamaguchi does not disclose or suggest a first determination section configured to determine a finished gate length Lg as recited in Applicants' independent Claims 7-8 or as disclosed in Applicants' originally filed specification.[6] Furthermore, Yamaguchi does not disclose or suggest a calculation section configured to plot an effective channel length Leff and a gate capacitance Cg so as to calculate a gradient A of a gate-

[1] Specification, page 7, line 20 – page 8, line 7.
[2] Yamaguchi, column 1, Field of Invention.
[3] Yamaguchi, column 10, line 55 – column13, line 15; Figure 4.
[4] Yamaguchi, column 16, lines 28-43.
[5] Yamaguchi, column 14, line 36 – column 15, line 3.
[6] Specification, page l, lines 8-16.

capacitance-vs.-effective-channel-length characteristics as recited in Applicants' Claim 7 or a calculation section configured to plot a design gate length Ld and a gate capacitance Cg to calculate a gradient A of a gate-capacitance-vs.-design-gate-length characteristics as recited in Applicants' Claim 8. In other words, Applicants' claimed inventions do not calculate or determine an effective channel width W_{eff} as disclosed in Yamaguchi.

Because Yamaguchi does not disclose or suggest all the elements of independent Claims 7-8, Applicants submit the inventions defined by Claims 7-8, and all claims depending therefrom, are not anticipated and are not rendered obvious by the asserted prior art for at least the reasons stated above.[7]

Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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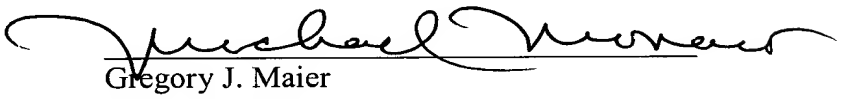

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[7] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."